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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/501,493	02/09/2000	John Marland Garth	ST9-99-130	3937

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EXAMINER	
VO, LILIAN	
ART UNIT	**PAPER NUMBER**
2195	

DATE MAILED: 09/20/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/501,493	GARTH ET AL.	
	Examiner	Art Unit	
	Lilian Vo	2195	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *05 July 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 57* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 - 57* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Claims 1 – 57 are pending.

Claim Rejections - 35 USC § 103

2. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

3. Claims 1, 5, 6, 20, 24, 25, 39, 43 and 44 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin "Resource Management System for Multimedia Devices" (hereinafter IBM Bulletin) in view of Arakawa et al. (US Pat. Application Publication 2002/0065793, hereinafter Arakawa).

4. Regarding **claims 1, 20, and 39**, IBM Bulletin discloses a method of processing data comprising the steps of:

identifying memory constraints (page 4, 1st paragraph: number of concurrently executing tasks is bounded by memory);

identifying processing capabilities (page 4, 1st paragraph: number of concurrently executing tasks is bounded by processor capabilities); and

determining a number of tasks to be started in parallel based on the identified memory constraints and processing capabilities (page 4, 1st paragraph: number of concurrently executing tasks is bounded by memory and processor capabilities).

IBM Bulletin did not disclose the tasks are the load and sort tasks. Nevertheless, Arakawa discloses of parallel processing, in which tasks such as sort processes and load processes performed in parallel (fig. 11, page 1, paragraph 12: executing parallel sorting processes at a plurality of computers. Page 6, paragraph 88. Page 7, paragraph 92: a process of storing a sorted string from plurality of input nodes to plurality of shared disk 500 is executed). Arakawa further discloses that parallel processing shortens a process time by preparing a plurality of resources necessary for information processing and performing a plurality of tasks at the same time, thereby attempting to reduce the processing time (page 1, paragraph 8). It would have obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate the load and sort functions/tasks of Arakawa together with IBM Bulletin to concurrently perform tasks such as loading the audio and/or midi tasks and sorting the tasks according to the size of the data/file to take advantage of high speed processing (Arakawa: page 1, paragraph 8) for performance enhancement and optimization.

5. Regarding **claim 5,** as modified IBM Bulletin discloses that the number of concurrently executing tasks is bounded by processor capabilities (IBM Bulletin, page 4, 1st paragraph: number of concurrently executing tasks is bounded by processor capabilities).

6. Regarding **claim 6**, as modified IBM Bulletin discloses that the number of concurrently executing tasks is bounded by processor memory (IBM Bulletin, page 4, 1st paragraph: number of concurrently executing tasks is bounded by memory).

7. **Claims 24 – 25 and 43 – 44** are rejected on the same ground as stated in claims 5 – 6 above.

8. Claims 2 – 3, 21 – 22, and 40 - 41 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin in view of Arakawa et al. (US Pat. Application Publication 2002/0065793) as applied to claims 1, 20, and 39 above, and further in view of Hintz et al. (US Pat 5,222,235, hereinafter Hintz).

9. Regarding **claim 2**, as modified IBM Bulletin did not teach the additional limitation as claimed. Nevertheless, the step determining a number of build processes based on the number of sort processes is considered common knowledge in the art per Hintz's invention (fig. 1, col. 3, line 46 – col. 4, line 7, col. 5, lines 50 - 51).

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to realize this common feature shown by Hintz to modified IBM Bulletin as one in the pertained art would know that build process is a consequential step directly dependent on sort process.

10. Regarding **claim 3**, as modified IBM Bulletin fails to teach the number of sort processes does not exceed a number of indexes to be built. Nevertheless, according to Hintz's teachings (col. 5, lines 50 - 51), "one index at a time" clearly indicates the claimed invention, in which the number of indexes excessive to the number of sort processes would not be possible.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate this feature as taught by Hintz to modified IBM Bulletin and to realize this common feature shown by Hintz as one in the pertained art would know that build process is a consequential step directly dependent on sort process and that it would not be possible for the number of sort processes to exceed a number of indexes to be built.

11. **Claims 21 – 22 and 40 – 41** are rejected on the same ground as stated in claims 2 – 3 above.

12. Claims 4, 23, and 42 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin in view of Arakawa et al. (US Pat. Application Publication 2002/0065793), as applied to claims 1, 20, and 39 above, and further in view of Bordonaro et al. (US Pat 5,307,485, hereinafter Bordonaro).

13. Regarding **claim 4,** ad modified IBM Bulletin did not teach the number of load processes does not exceed a number of partitions to be loaded. Nevertheless, this feature has been taught by Bordonaro (fig. 3, 310 shows N partitioned tasks and 312 distributes over the N processors). In fig. 2, 202 shows that as the records from storage device are loaded, col. 4, line 62 – col. 6,

line 27 describes the fact that N partitioned tasks corresponds to N processors, which implies the limitation, in which the number of load processes does not exceed a number of partitions to be loaded. Note that fig. 2 corresponds to fig. 3 in that records loaded into memory are to be part of the portion from which tasks are created (col. 5, lines 58 – 60) and subsequently, divided in to partitions for load processes, as shown in fig. 3.

It would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate the feature as taught by Bordonaro to modified IBM Bulletin so that various memory constraints would still be suitable to apply the desired processes (Bordonaro: col. 1, lines 33 – 56).

14. **Claims 23 and 42** are rejected on the same ground as stated in claim 4 above.

15. Claims 7 – 11, 26 – 30 and 45 - 49 are rejected under 35 U.S.C. 103(a) as being unpatentable over IBM Technical Disclosure Bulletin in view of Arakawa et al. (US Pat. Application Publication 2002/0065793), as applied to claims 1, 20, and 39 above, and further in view of an "Official Notice".

16. Regarding **claims 7 – 11, 26 – 30, and 45 – 49**, as modified IBM Bulletin did not teach the additional limitations as claimed. Nevertheless, the examiner takes an "Official Notice" that the limitations narrowed by these claims are considered obvious and furthermore a matter of design choice, since applicants have not disclosed that the claimed limitations solve any stated problem or are for any particular purpose and it appears that the invention would perform equally

well without the claimed features. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to efficiently utilize all the processing capabilities required for the desired task.

Allowable Subject Matter

17. **Claims 12 – 19, 31 – 38, and 50 - 57** are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

18. Applicant's arguments filed 7/5/05 have been fully considered but they are not persuasive for the reasons set forth below.

19. Regarding applicant's remark that IBM and Arakawa references when combine, do not teach or suggest the limitations of claim 1 (page 17, 7th paragraph), the examiner disagrees. For instance, IBM reference discloses the step of identifying memory constraints (page 4, 1st paragraph: number of concurrently executing tasks is bounded by memory), identifying processing capabilities (page 4, 1st paragraph: number of concurrently executing tasks is bounded by processor capabilities), and determining a number of tasks to be started in parallel based on the identified memory constraints and processing capabilities (page 4, 1st paragraph: number of concurrently executing tasks is bounded by memory and processor capabilities).

IBM Bulletin did not disclose the tasks are the load and sort tasks. Nevertheless, Arakawa discloses of parallel processing, in which tasks such as sort processes and load processes performed in parallel (fig. 11, page 1, paragraph 12: executing parallel sorting processes at a plurality of computers. Page 6, paragraph 88. Page 7, paragraph 92: a process of storing a sorted string from plurality of input nodes to plurality of shared disk 500 is executed). Arakawa further discloses that parallel processing shortens a process time by preparing a plurality of resources necessary for information processing and performing a plurality of tasks at the same time, thereby attempting to reduce the processing time (page 1, paragraph 8). It would have obvious for one of an ordinary skill in the art, at the time the invention was made, to incorporate the load and sort functions/tasks of Arakawa together with IBM Bulletin to concurrently perform tasks such as loading the audio and/or midi tasks and sorting the tasks according to the size of the data/file to take advantage of high speed processing (Arakawa: page 1, paragraph 8) for performance enhancement and optimization.

20. In response to applicant's argument that there is no suggestion to combine the references (page 17, 8th paragraph), the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988) and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, the motivation for the rejection is found in the reference, Arakawa, page 1, paragraph 8.

21. In response to applicant's argument that the examiner's conclusion of obviousness is based upon improper hindsight reasoning (page 17, 8th paragraph), it must be recognized that any judgment on obviousness is in a sense necessarily a reconstruction based upon hindsight reasoning. But so long as it takes into account only knowledge which was within the level of ordinary skill at the time the claimed invention was made, and does not include knowledge gleaned only from the applicant's disclosure, such a reconstruction is proper. See *In re McLaughlin*, 443 F.2d 1392, 170 USPQ 209 (CCPA 1971).

22. In response to applicant's argument that the combination of IBM and Arakawa do not renders obvious (page 17, 7th paragraph) and there can be no expectation of success from the combination (page 17, last paragraph), the test for obviousness is not whether the features of a secondary reference may be bodily incorporated into the structure of the primary reference; nor is it that the claimed invention must be expressly suggested in any one or all of the references. Rather, the test is what the combined teachings of the references would have suggested to those of ordinary skill in the art. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981).

23. In response to applicant's argument that claims 2 - 6, 21 –25 and 40 – 45 recite additional novel elements not shown by the references (page 18, 4th paragraph – page 19, 3rd paragraph), a recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed

invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

Regarding applicant's argument with respect to claims 2, 21 and 40 (page 18, 5th paragraph), Hintz suggests the step determining a number of build processes based on the number of sort processes in fig. 1, col. 3, line 46 – col. 4, line 7 and col. 5, lines 50 - 51. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to realize this common feature shown by Hintz to modified IBM Bulletin as one in the pertained art would know that build process is a consequential step directly dependent on sort process.

Regarding applicant's argument with respect to claims 3, 22 and 41 (page 18, 6th paragraph), Hintz suggests the number of sort processes does not exceed a number of indexes to be built in col. 5, lines 50 - 51, as he discloses "one index at a time" in which the number of indexes excessive to the number of sort processes would not be possible. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate this feature as taught by Hintz to modified IBM Bulletin and to realize this common feature shown by Hintz as one in the pertained art would know that build process is a consequential step directly dependent on sort process and that it would not be possible for the number of sort processes to exceed a number of indexes to be built.

Regarding applicant's argument with respect to claims 4, 23 and 42 (page 18, 7th paragraph), Bordonaro suggests the number of load processes does not exceed a number of partitions to be loaded in fig. 3, 310, which shows N partitioned tasks and 312 distributes over the N processors. In fig. 2, 202 shows that as the records from storage device are loaded, col. 4,

line 62 – col. 6, line 27 describes the fact that N partitioned tasks corresponds to N processors, which implies the limitation, in which the number of load processes does not exceed a number of partitions to be loaded. Note that fig. 2 corresponds to fig. 3 in that records loaded into memory are to be part of the portion from which tasks are created (col. 5, lines 58 – 60) and subsequently, divided in to partitions for load processes, as shown in fig. 3. Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate the feature as taught by Bordonaro to modified IBM Bulletin so that various memory constraints would still be suitable to apply the desired processes (Bordonaro: col. 1, lines 33 – 56).

Regarding applicant's argument with respect to claims 5, 24 and 43 (page 19, 1st paragraph), as modified IBM clearly suggests the number of concurrently executing tasks is bounded by processor capabilities (IBM Bulletin, page 4, 1st paragraph: number of concurrently executing tasks is bounded by processor capabilities). As stated above, tasks here also include sort processes as well as load processes.

Regarding applicant's argument with respect to claims 6, 25and 44 (page 19, 2nd paragraph), as modified IBM clearly suggests the number of concurrently executing tasks is bounded by processor memory (IBM Bulletin, page 4, 1st paragraph: number of concurrently executing tasks is bounded by memory).

Conclusion

24. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

25. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Lilian Vo whose telephone number is 571-272-3774. The examiner can normally be reached on Monday - Thursday, 7:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng-Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR

system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Lilian Vo
Examiner
Art Unit 2195

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September 15, 2005

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